REMARKS

By this Amendment, claims 1, 5-6, 9, 14 and 19 are amended. Claims 7-8, 10-13, 15-18 and 20 remain in the application. Thus, claims 1 and 5-20 are active in the application. Reexamination and reconsideration of the application are respectfully requested.

Minor editorial revisions were made to the substitute specification in order to correct idiomatic and typographical errors therein. No new matter was added via the editorial revisions to the specification.

In item 1 on page 2 of the Office Action, claim 1 was objected to because the term "patters" in line 6 should read "patterns." Claim 1 has been revised to replace the term "patters" in line 6 with the term "patterns," as kindly suggested by the Examiner. Accordingly, the Applicant respectfully requests the objection of claim 1 to be withdrawn.

In item 2 on page 2 of the Office Action, claims 1, 9 and 14, as well as the claims depending therefrom, were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. The Examiner asserted that these claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use or the invention.

In particular, the Examiner asserted that the recitation in claim 1 of the dummy patterns being formed in "standard areas," the recitation in claim 9 of the dummy patterns having a "standard rectangular outline and being arranged in a matrix with predetermined spacing," and the recitation in claim 14 of the dummy patterns being formed in a plurality of "standard areas arranged in a matrix with predetermined spacing" are not supported by the specification.

The limitation "standard areas" defines dummy areas each having the same shape. Similarly, the limitation "each of said plurality of dummy patterns having a standard rectangular outline" defines each of the plurality of dummy patterns as having a rectangular outline which are equal in shape to each other. The present invention clearly provides support for the plurality of dummy areas each having the same shape and the

plurality of dummy patterns each having a rectangular outline which is equal in shape to each other in the illustrations of Figures 1(A), 3(A), 4(A) and 5(A).

In view of the Examiner's objection to the usage of the term "standard area" or "standard rectangular outline," claims 1, 9 and 14 have each been revised so as to define the inventions of these claims in view of the illustrations of Figures 1(A), 3(A), 4(A) and 5(A), which, as described above, clearly provide support for the plurality of dummy areas each having the same shape and the plurality of dummy patterns each having a rectangular outline which is equal in shape to each other.

In particular, claim 1 has been amended to recite that the plurality of dummy patterns are "formed within a plurality of dummy areas each having a same shape." Claim 9 has been amended to recite that each of the plurality of dummy patterns has "a same rectangular outline as each other" and is "arranged in a matrix with predetermined spacing." Claim 14 has been amended to recite that the plurality of dummy patterns are formed in "a plurality of dummy areas each having a same shape and being arranged in a matrix with predetermined spacing."

The revised limitations of claims 1, 9 and 14 are clearly supported by the Applicant's specification, specifically the illustrations of Figures 1(A), 3(A), 4(A) and 5(A). The Applicant notes that the Examiner, on page 6 of the Office Action, contends that claim 9 recites "wherein each of said plurality of dummy patterns has a space portion [an opening] within each of the standard areas so that a pattern ratio of said semiconductor device is reduced." The Applicant submits, however, that the underlined portion of the above quotation is not recited in claim 9. Nonetheless, the Applicant submits that the specification clearly provides support for each of the plurality of dummy patterns having an opening so that a pattern ratio of the semiconductor device is reduced. For example, the specification clearly describes, in lines 13-17 on page 9 of the substitute specification (lines 5-9 on page 10 of the original specification), that the provision of the slits (opening) at the dummy patterns reduces a pattern ratio of the semiconductor device.

Accordingly, in view of the above amendments and remarks, the Applicant respectfully requests the Examiner to withdraw the rejection of claims 1, 9 and 14, as well as the claims depending therefrom, under 35 U.S.C. § 112, first paragraph.

In item 3 on page 3 of the Office Action, claims 1, 6 and 14 were rejected under 35 U.S.C. § 102(b) as being anticipated by Motoyama et al. (U.S. 6,099,992). Furthermore, in item 4 on page 5 of the Office Action, claims 5, 7-10 and 19-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Motoyama et al.

These rejections are respectfully traversed for the following reasons.

The present invention provides a semiconductor device having a plurality of dummy patterns. As shown in Figures 1(A), 3(A), 4(A) and 5(A), the plurality of dummy patterns of the present invention are formed in dummy areas, or the dummy patterns have a same rectangular outline as each other and are arranged in a matrix with predetermined spacing. A plurality of dummy line patterns (Figure 1(A)) or a single pattern with an opening (Figures 3(A), 4(A), 5(A)) are formed in the plurality of dummy areas. Accordingly, since the dummy areas each have a space portion, i.e., a space between the line patterns or the opening, a pattern ratio of the semiconductor device is reduced. Therefore, as described, for example, in lines 8-13 on page 9 of the substitute specification (lines 5-9 on page 10 of the original specification), an advantageous effect of the present invention is that it is possible to more effectively suppress an increase in the global step.

Independent claims 1, 9 and 14 each recite the semiconductor device of the present invention as having the above-described features.

Claim 1 recites a semiconductor device which comprises a semiconductor substrate having a pattern forming region and a pattern non-forming region, and a wiring pattern formed on the pattern forming region. The semiconductor device of claim 1 also comprises a plurality of dummy patterns formed on the pattern non-forming region, where the plurality of dummy patters are formed within a plurality of dummy areas, and an insulating film formed on the wiring pattern and the plurality of dummy patterns. As defined in claim 1, each of the plurality dummy patterns is spaced apart with a width filled by plus sizing of the insulating film formed on the plurality of dummy patterns.

Claim 9 recites a semiconductor device which comprises a semiconductor substrate having a pattern area and a non-pattern area, and a conductive pattern formed on the pattern area of the semiconductor substrate. The semiconductor device of claim 9 also comprises a plurality of dummy patterns formed on the non-pattern area of the

semiconductor substrate, where each of the plurality of dummy patterns has a same rectangular outline and is arranged in a matrix with predetermined spacing. As defined in claim 9, each of the plurality of dummy patterns has an opening so that a pattern ratio of the semiconductor device is reduced.

Claim 14 recites a semiconductor device which comprises a semiconductor substrate having a pattern area and a non-pattern area, a conductor pattern formed on the pattern area of the semiconductor substrate, and a plurality of dummy patterns formed on the non-pattern area of the semiconductor substrate. As defined in claim 14, each of the plurality of dummy patterns are formed in a plurality of dummy areas each having a same shape and being arranged in a matrix with predetermined spacing, and each of the plurality of dummy patterns has a space portion within each of the standard areas so that a pattern ratio of the semiconductor device is reduced.

Motayama et al. discloses a semiconductor device in which interconnection patterns 21 are laid on a substrate, and first dummy patterns 22 are disposed at a fixed interval W from the interconnection patterns 21 (see Column 7, lines 26-29 and Figure 5A). A lattice-like pattern 23 is then laid onto the first dummy patterns 22, and the portions of the first dummy patterns which are disposed under the lattice-like (reticular) pattern 23 are removed to form second (divided and separated) dummy patterns 22d-22h (see Column 7, lines 30-39 and Figures 5B-5C).

Motyama et al. also discloses that the widths of the second dummy patterns 22d-22h are measured to find whether or not any of the widths thereof fall short of the smallest allowable width "a". If any of the second dummy patterns 22d-22h are determined to have a width smaller than the smallest allowable width (i.e., dummy patterns 22e-22f in Figure 5C), a third dummy pattern 22i which was removed as being disposed under the lattice-like pattern 23 are restored by being adjoined to the dummy patterns 22e-22f so as to ensure that each of the restored second dummy patterns 22e-22f have a width equal to or larger than the smallest allowable width (see Column 7, lines 47-67 and Figures 5C-5D).

Motoyama et al. discloses that after the widths of the second dummy patterns 22d-22h are determined and restored if smaller than the smallest allowable width, the areas of the second dummy patterns 22d, 22g, 22h are measured to determine if whether or not

any of the second dummy patterns has an area which is smaller than the smallest allowable area, S. If any of the second dummy patterns has an area smaller than the smallest allowable area, the third dummy pattern 221 which was removed as being disposed under the lattice-like pattern 23 are restored by being adjoined to the second dummy patterns having the smaller than allowable area in a manner similar to the process of restoring the second dummy patterns 22e-22f to have an allowable width (see Column 8, lines 1-27 and Figures 5D-5E).

Accordingly, Motayama et al. discloses a semiconductor device having dummy patterns. Motayama et al. also discloses that all of the areas including pattern areas and non-pattern areas are divided into standard areas by using the lattice-like pattern 23, as shown in Figure 5B.

However, Motayama et al. clearly does not disclose or suggest that a single dummy pattern or a plurality of dummy patterns with an opening is/are formed in each of the dummy areas having a same shape as each other. That is, as shown, for example, by arrow 1.65 in Figure 7A, a single dummy pattern without an opening or space portion is formed in each dummy area, and there is only a single dummy pattern in each dummy area.

Accordingly, Motayama et al. clearly does not disclose or suggest that each of the plurality dummy patterns is spaced apart with a width filled by plus sizing of the insulating film formed on the plurality of dummy patterns, as recited in claim 1. Similarly, Motayama et al. clearly does not disclose or suggest that each of the plurality of dummy patterns has an opening so that a pattern ratio of the semiconductor device is reduced, as recited in new claim 9. Moreover, Motayama et al. clearly does not disclose or suggest that each of the plurality of dummy patterns has a space portion within each of the standard areas so that a pattern ratio of the semiconductor device is reduced, as recited in new claim 14.

Accordingly, Motayama et al. clearly does not disclose or suggest each and every limitation of claims 1, 9 and 14.

Therefore, claims 1, 9 and 14 are clearly not anticipated or rendered obvious by Motayama et al. since Motayama et al. fails to disclose each and every limitation of claims 1, 9 and 14. Accordingly, it is submitted that the claims 1, 9 and 14, as well as

claims 5-8, 10-13 and 15-20 which depend therefrom, are clearly allowable over the prior art as applied by the Examiner.

In view of the foregoing amendments and remarks, it is respectfully submitted that the present application is clearly in condition for allowance. An early notice thereof is respectfully solicited.

If, after reviewing this Amendment, the Examiner feels there are any issues remaining which must be resolved before the application can be passed to issue, the Examiner is respectfully requested to contact the undersigned by telephone in order to resolve such issues.

Respectfully submitted,

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